Midterm Exam

(October 16th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (20 PTS)

• Compute the result of the following operations. The operands are signed fixed-point numbers. The result must be a signed fixed point number. For the division, use x = 5 fractional bits.

1.0111 +	1.010101 -	01.11111 +							
1.101001	1000.0101	0.10001							
10.101 ×	1.001 ×	10.1010 ÷							
1.01101	0.1011	0.101							

PROBLEM 2 (30 PTS)

• Calculate the result (provide the 32-bit result) of the following operations with single floating point numbers. Truncate the results when required. When doing fixed-point division, use x = 4 fractional bits.

✓ C0D00000 + 42EA	0000 ✓ 50A90000 - 4F480000	✓ 80400000 × 7AB80000	✓ FB380000 ÷ 48C00000

PROBLEM 3 (13 PTS)

• Convert the following signed fixed point numbers in format [12 8] to the dual fixed point format 12_8_4.

		3 3 1			
	FX	A.D7	F.AE	7.1F	8.C4
	DFX				

PROBLEM 4 (22 PTS)

Calculate the result of the following operations where the numbers are represented in dual fixed-point arithmetic (12_8_4).
 Note that the results must be in the same format. Include an overflow bit when necessary.

DFX Format 12_8_4	Result	Overflow		Result	overflow
FAC + 7EE			10A-C0A		
40B + 78B			999-674		

PROBLEM 5 (15 PTS)

• Complete the timing diagram of the following iterative unsigned multiplier (N = 4, M = 4). Register: *sclr*: synchronous clear. Here, if *sclr* = E = 1, the register contents are initialized to 0. Parallel access shift register: If E = 1: $s_l = 1 \rightarrow \text{Load}$, $s_l = 0 \rightarrow \text{Shift}$

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ITERATIVE MULTIPLIER		DB	clock	$ \rightarrow $					ſĽ	♪ Ľ		
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요 나	0→din 0→	Ó♥ din	DA		1001		 	1	1	1	1	i
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$s \rightarrow EP$	Shift-left	Shift-righ	nt				 	 	1	1	1	1
$b_{0} \rightarrow FSM \rightarrow done$	8	4	S		ן ון	1	I		<u> </u>	<u>i</u>	<u>i</u> !	į
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	♥ ₽		Е	į			 	1	1		 	į
	, 0		sclrP				 		1			Ì
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